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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SHINGLETON, MICHAEL B	

ART UNIT	PAPER NUMBER
2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,263	SENTHILKUMAR ET AL.	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19,35-39,41-45 and 47-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,35-39,41-45 and 47-53* is/are rejected.

7)☒ Claim(s) *54 and 55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7-5-2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Plangger et al. 4,582,434 (Plangger) in view of Clarke US 6,337,604 (Clarke).

Figures 1 and 2 of Plangger provides for the claimed method steps and apparatus structure that includes the step of generating a system time signal using a real time clock circuit composed of at least element 104 that has a tunable oscillator composed of at least element 98 for adjusting an operation frequency of the real time clock circuit. The system time signal is internal to the data processor 80 (See column 7). This processor receives a reference time signal data over a network. The particular network that Plangger uses happens to be the WWV network. The examiner must give the broadest reasonable interpretation to the claimed invention consistent with the specification. It is accordingly noted that applicant has not defined the term "network" in the specification and thus the common everyday definition of this term applies. Plangger clearly describes in column 8 how the variable capacitance element 98 of the tunable oscillator is controlled so as to adjust the tunable oscillator in order to increase or decrease the operating frequency of the real time clock circuit in response to a difference between the system time signal and the reference time signal. Plangger utilizes a single adjustable capacitor namely a varactor diode 98 to vary the capacitance of the tunable oscillator that generates the real time clock signal used by the processor. Claim 19 recites a set of control signals to modify the selection of a set of capacitors within a capacitor bank so as to from a variable capacitor used in the real time clock circuit that in turn whose variations correlates to the changes in operation frequency of the real time clock circuit. As evidenced by Clarke, one art recognized variable capacitance structure that is used to control the frequency of an oscillator that is used as a clock is the plurality of independently selectable on-chip capacitors (Note elements C1-C6 and the corresponding control signal D_o-D_5.). Applicant has added by way of the amendment dated 7-5-2005 limitations that require the "initializing a set of control signals" and eliminated limitations like requiring MOSFET capacitors. This in effect broaden the claims over what they were previously for Plangger clearly recites in column 7 around line 63 the initializing of a set

for control signals that is latched into the latch circuit 91. The initial value is the "number 127". Plangger is silent on how these control signals representing the number 127 is stored or set when the circuit is first initialized.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the variable capacitor of Plangger with one that is composed of a plurality of capacitors each switched by a control circuit like that of Clarke given the art recognized equivalence of these two capacitor arrangements as taught by Clarke. Also one of ordinary skill in the art additionally would have been motivated to replace the variable capacitor arrangement of Plangger with that of a switch combination of capacitors because it is well-known that the switched combination of capacitors do not require a digital to analog converter and thus elements like 92 and 93 could be eliminated in Plangger.

Claims 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Plangger et al. 4,582,434 (Plangger) in view of Clarke US 6,337,604 (Clarke) as applied to claim 19 above, and further in view of Klughart US 5,8701,411 (Klughart '411).

Plangger and Clarke are also silent on the use of on chip p-type enhancement MOSFET capacitors for the capacitors that make up the bank of capacitors.

Figure 9b of Klughart '411 discloses the use of on-chip p-enhancement MOSFET capacitor 32 whose source and drain are clearly connected together as "common" i.e. conventional (See column 7, around line 18). Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '411.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip p-enhancement MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors Clarke because, as the Clarke reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known on-chip p-enhancement MOSFET capacitors as recited by Klughart '411.

Plangger, Clarke and Klughart '411 are silent on the use of a filter capacitor i.e. low pass filter so to generate a filtered DC voltage signal to bias the capacitors of the oscillator contains the bias signal and no other unwanted signals like noise, AC components etc..

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted a conventional constant voltage circuit that includes a filter capacitor for the constant voltage circuit of Clarke because, as the reference is silent as to the exact composition of the constant voltage circuit one of ordinary skill in the art would have been motivated to use any art-recognized equivalent constant voltage circuit such as the well-known constant voltage circuit that includes a filter capacitor.

Claims 35, 44, 47-50 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Plangger et al. 4,582,434 (Plangger) in view of Clarke US 6,337,604 (Clarke) and Park 6,804,775 (Park).

Figures 1 and 2 of Plangger provides for the claimed method steps and apparatus structure that includes the step of generating a system time signal using a real time clock circuit composed of at least element 104 that has a tunable oscillator composed of at least element 98 for adjusting an operation frequency of the real time clock circuit. The system time signal is internal to the data processor 80 (See column 7). This processor receives a reference time signal data over a network. The particular network that Plangger uses happens to be the WWV network. The examiner must give the broadest reasonable interpretation to the claimed invention consistent with the specification. It is accordingly noted that applicant has not defined the term "network" in the specification and thus the common everyday definition of this term applies. Plangger clearly describes in column 8 how the variable capacitance element 98 of the tunable oscillator is controlled so as to adjust the tunable oscillator in order to increase or decrease the operating frequency of the real time clock circuit in response to a difference between the system time signal and the reference time signal. Plangger utilizes a single adjustable capacitor namely a varactor diode 98 to vary the capacitance of the tunable oscillator that generates the real time clock signal used by the processor. Claim 19 recites a set of control signals to modify the selection of a set of capacitors within a capacitor bank so as to from a variable capacitor used in the real time clock circuit that in turn whose variations correlates to the changes in operation frequency of the real time clock circuit. As evidenced by Clarke, one art recognized variable capacitance structure that is used to control the frequency of an oscillator that is used as a clock is the plurality of independently selectable on-chip capacitors (Note elements C1-C6 and the corresponding control signal D_0-D_5.). Applicant has added by way of the amendment dated 7-5-2005 limitations that require the "initializing a set of control signals" and eliminated limitations like requiring MOSFET capacitors. This in effect broaden the claims over what they were previously for Plangger clearly recites in column 7 around line 63 the initializing of a set for control signals that is latched into the latch circuit 91. The initial value is the "number 127". Plangger

is silent on how these control signals representing the number 127 is stored or set when the circuit is first initialized.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the variable capacitor of Plangger with one that is composed of a plurality of capacitors each switched by a control circuit like that of Clarke given the art recognized equivalence of these two capacitor arrangements as taught by Clarke. Also one of ordinary skill in the art additionally would have been motivated to replace the variable capacitor arrangement of Plangger with that of a switch combination of capacitors because it is well-known that the switched combination of capacitors do not require a digital to analog converter and thus elements like 92 and 93 could be eliminated in Plangger.

Plangger and Clarke are silent on the use of a BIOS arrangement to boot up the processor.

Column 3 around line 15 of Park recites the commonly known usages for a BIOS which includes the adjusting of the system clock otherwise known as the real time clock of the crystal oscillator of the micro-processor arrangement. It is conventionally known that BIOS clearly includes memory (register) to store the initial values that BIOS uses to set or adjust hardware items in a processor arrangement like the system clock.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a BIOS in Plangger to store and set the values for initializing the "logic circuit" because as the Plangger reference is silent on the exact structure that causes the initialization values to be stored an used at initialization one of ordinary skill in the art would have been motivated to use any art-recognized equivalent initialization means such as the conventional BIOS arrangement as taught by Park.

The combination above is silent on the exact values of the capacitors that make up the capacitor bank. Specifically having one that is less than 1 pF.

However, the selection of the capacitance values is merely part of the optimum or workable range. The values of the capacitors determines how many are needed and how great a resolution one can obtain which is all part of the selection of optimum or workable range.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have selected the value of at least one of the capacitances to be less than one pico-Farad (PF) as this is the selection of the optimum or workable range that involves but routine skill in the art. One of ordinary skill in the art would have been motivated to make the combination because this selection of the

value of the capacitance is merely the discovering of an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

The combination above is silent on the use of non-volatile memory (storage) for the memory of the BIOS as taught by Park. Non-volatile memory is a well-known art recognized equivalent form of memory used in a BIOS. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the memory of Park in the combination made obvious above with non-volatile memory because as the Plangger, Clarke and Park references are silent on the exact structure of the memory for the initial values one of ordinary skill in the art would have been motivated to use any art-recognized equivalent memory for storage of the initial values such as the conventional non-volatile memory (storage). Claim 49 recite that the BIOS arrangement "evaluates" the values stored in memory to determine whether to initialize the real time claims based on the values in the BIOS. Evaluate is in the broad sense is "to determine the value of". This is thus seen as a very broad limitation that the BIOS in Park covers. In other words, the memory in the BIOS is evaluated by the program and sub-program of the BIOS to be within a determined value, i.e. it must lie within the range which the program and/or sub-program is programmed to handle and if it is within the acceptable range of values the boot-up of the system clock will occur at the initial value specified by the BIOS memory.

Claims 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Plangger et al. 4,582,434 (Plangger) in view of Clarke US 6,337,604 (Clarke) and Park 6,804,775 (Park) as applied to claims 35, 44, 47-50 and 53 above, and further in view of Klughart US 5,546,055 (Klughart '055).

In additional to that applied to claims 35, 44, 47-50 and 53 above Figures 1 and 2 of Plangger provides for the claimed method steps and apparatus structure that includes the step of generating a system time signal using a real time clock circuit composed of at least element 104 that has a tunable oscillator composed of at least element 98 for adjusting an operation frequency of the real time clock circuit. The system time signal is internal to the data processor 80 (See column 7). This processor receives a reference time signal data over a network. The particular network that Plangger uses happens to be the WWV network. The examiner must give the broadest reasonable interpretation to the claimed invention consistent with the specification. It is accordingly noted that applicant has not defined the term "network" in the specification and thus the common everyday definition of this term applies. Plangger clearly describes in column 8 how the variable capacitance element 98 of the tunable oscillator is controlled so as to adjust the tunable oscillator in order to increase or decrease the operating frequency of the real time clock circuit in response to a difference between the system time signal and the reference time signal. Plangger utilizes a single adjustable capacitor namely a varactor diode 98 to vary the capacitance of the tunable oscillator that generates the real time clock signal used by the processor. Claim

19 recites a set of control signals to modify the selection of a set of capacitors within a capacitor bank so as to from a variable capacitor used in the real time clock circuit that in turn whose variations correlates to the changes in operation frequency of the real time clock circuit. As evidenced by Clarke, one art recognized variable capacitance structure that is used to control the frequency of an oscillator that is used as a clock is the plurality of independently selectable on-chip capacitors (Note elements C1-C6 and the corresponding control signal D_0-D_5.). Applicant has added by way of the amendment dated 7-5-2005 limitations that require the "initializing a set of control signals" and eliminated limitations like requiring MOSFET capacitors. This in effect broaden the claims over what they were previously for Plangger recites in column 7 around line 63 the initializing of a set for control signals that is latched into the latch circuit 91. The initial value is the "number 127". Plangger is silent on how this number 127 is stored or set when the circuit is first initialized.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the variable capacitor of Plangger with one that is composed of a plurality of capacitors each switched by a control circuit like that of Clarke given the art recognized equivalence of these two capacitor arrangements as taught by Clarke. Also one of ordinary skill in the art additionally would have been motivated to replace the variable capacitor arrangement of Plangger with that of a switch combination of capacitors because it is well-known that the switched combination of capacitors do not require a digital to analog converter and thus elements like 92 and 93 could be eliminated in Plangger.

Plangger and Clarke are also silent on the use of MOSFET capacitors for the capacitors that make up the bank of capacitors.

Figure 9 of Klughart '055 discloses the use of on-chip n-depletion MOSFET load capacitors 1230 and 1232 whose source and drain are clearly connected together as is clearly illustrated. Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '055.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip n-depletion MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors of the combination made obvious above wherein each of these capacitors has a terminal connected to ground given the art recognized equivalents of these capacitor arrangements. as taught by Klughart '055.

Plangger, Clarke and Klughart are silent on the use of a filter capacitor i.e. low pass filter so to generate a filtered DC voltage signal to bias the capacitors of the oscillator contains the bias signal and no other unwanted signals like noise, AC components etc..

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted a conventional constant voltage circuit that includes a filter capacitor for the constant voltage circuit of Clarke because, as the reference is silent as to the exact composition of the constant voltage circuit one of ordinary skill in the art would have been motivated to use any art-recognized equivalent constant voltage circuit such as the well-known constant voltage circuit that includes a filter capacitor.

Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Plangger et al. 4,582,434 (Plangger), Clarke US 6,337,604 (Clarke), Park 6,804,775 (Park) and Klughart US 5,546,055 (Klughart '055) as applied to claims 35-37, 44, 47-50 and 53 above, and further in view of Horn "Basic Electronics Theory" 4th Edition pp 377-378, pp 418-426 and pp 454-465.

In additional to that applied to claims 35, 37, 44, 47-50 and 53 above and the following: Plangger and Clarke are silent on using buffer circuitry to decouple the switches from the set of memory registers.

Horn teaches that buffers are used to ensure that the output drive is sufficient to drive the devices on the output thereof.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a buffers between the transmission gate switches and the memory registers so as to insure that there is sufficient drive for the transmission gate switches as taught by Horn.

Clarke is likewise silent on the use of filtered power signals to power the buffer circuitry. Buffer circuitry requires a power supply as is well known in the art so that it can provide the sufficient drive as noted above. Horn teaches that it is commonplace to utilize filtered power supplies, in particular note pages 456 and 460 to power electronic devices. This as Horn recognizes reduces "ripple", i.e. noise, or voltage fluctuations that then in turn causes less vacillations in the devices powered by such power supplies.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a filtered power supply to power the buffers made obvious above so as to reduce the introduction of noise in the system as is taught by Horn.

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Plangger et al. 4,582,434 (Plangger) in view of Clarke US 6,337,604 (Clarke) and Park 6,804,775 (Park) as applied to claims 35, 44, 47-50 and 53 above, and further in view of Kuhn Jr. US 3,930,169 (Kuhn, Jr.).

Clarke is silent on the composition of the switches 9, 11, 13, 15, 17, 19(a,b) that switches the capacitors in and out of the circuit so as to change the frequency of the oscillator.

Transmission gate switches are conventional switching means as noted by Kuhn, Jr. (See Figure 1 and column 4, lines 3-29).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted conventional transmission gate switches in place of the generic switches of Clarke because, as the reference is silent as the exact switching element employed one of ordinary skill in the art would have been motivated to use any art-recognized equivalent switch such as the well-known, conventional transmission gate switch as taught by Kuhn, Jr..

Note that the circuit of Clarke has a "set of registers" 21 to provide the control signals D0-D5 for selecting the individual capacitors C1-C6.

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable Plangger, Clarke, Park and Kuhn, Jr. as applied to claims 35, 41, 44, 47-50 and 53 above, and further in view of Horn "Basic Electronics Theory" 4th Edition pp 377-378, pp 418-426 and pp 454-465.

Clarke is silent on using buffer circuitry to decouple the transmission gate switches from the set of memory registers.

Horn teaches that buffers are used to ensure that the output drive is sufficient to drive the devices on the output thereof.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a buffers between the transmission gate switches and the memory registers so as to insure that there is sufficient drive for the transmission gate switches as taught by Horn.

As it relates to claim 10, Clarke is likewise silent on the use of filtered power signals to power the buffer circuitry. Buffer circuitry requires a power supply as is well known in the art so that it can provide the sufficient drive as noted above. Horn teaches that it is commonplace to utilize filtered power supplies, in particular note pages 456 and 460 to power electronic devices. This as Horn recognizes reduces "ripple", i.e. noise, or voltage fluctuations that then in turn causes less vacillations in the devices powered by such power supplies.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a filtered power supply to power the buffers made obvious above so as to reduce the introduction of noise in the system as is taught by Horn.

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Plangger et al. 4,582,434 (Plangger) in view of Clarke US 6,337,604 (Clarke) and Park 6,804,775 (Park) as applied to claims 35, 44, 47-50 and 53 above, and further in view of Klughart US 5,8701,411 (Klughart '411).

Plangger and Clarke are also silent on the use of on chip p-type enhancement MOSFET capacitors for the capacitors that make up the bank of capacitors.

Figure 9b of Klughart '411 discloses the use of on-chip p-enhancement MOSFET capacitor 32 whose source and drain are clearly connected together as "common" i.e. conventional (See column 7, around line 18). Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '411.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip p-enhancement MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors Clarke because, as the Clarke reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known on-chip p-enhancement MOSFET capacitors as recited by Klughart '411.

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Plangger et al. 4,582,434 (Plangger) in view of Clarke US 6,337,604 (Clarke) and Park 6,804,775 (Park). as applied to claims 35, 44, 47-50 and 53 above, and further in view of Klughart US 5,546,055 (Klughart '055).

Plangger and Clarke are also silent on the use of source-drain connected MOSFET capacitors for the capacitors that make up the bank of capacitors.

Figure 9 of Klughart '055 discloses the use of on-chip n-depletion MOSFET load capacitors 1230 and 1232 whose source and drain are clearly connected together as is clearly illustrated. Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '055.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip n-depletion MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in

place of the generic capacitors of the combination made obvious above wherein each of these capacitors has a terminal connected to ground given the art recognized equivalents of these capacitor arrangements. as taught by Klughart '055.

Claims 54 and 55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
August 4, 2005

Michael B Shingleton
Primary Examiner
Group Art Unit 2817